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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/606,582
Filing Date: June 26, 2003
Appellant(s): DAY ET AL.

Bradley D. Ellis
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 03/03/08 appealing from the Office action mailed 07/11/07

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Final Rejection

The appellant's statement of the status of the final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The drawing, 35 U.S.C. 112, first paragraph, and the 35 U.S.C. 101 rejections have been withdrawn by the examiner.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,408,354	Young	06-2002
6,801,972	Stuber	10-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 20-35**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Young (US pat. 6,408,354) in view of Stuber et al. (US pat. 6,801,972).

12. As per **claims 20 and 28**, Young discloses "A method for tracking communications between a processing unit (PU) **(bi-directional data channel 303 of fig. 3, as discloses in col. 7, line 12)** and an external device (ED) **(SCSI module 230 of fig. 3, as discloses in col. 7, line 14)**, comprising:

receiving, by the PU, data from the ED, into a read register **(bi-directional data buffer 340 of fig. 3) (see col. 7, lines 56-59, which discloses, "a first counter is incremented as each unit of data is transferred to bi-directional buffer 340". See**

fig. 3, which shows data is being transferring from the SCSI module to the buffer. See col. 5, lines 19-26 for further detail);

sending, by the PU, data to the ED, from a write register **(bi-directional data buffer 345 of fig. 3) (see col. 7, lines 17-18, which discloses, "at the same time that data is being received from SCSI bus 120 by buffer 345")**;

incrementing a read channel count upon receipt of inbound data from the ED by the PU**(see fig. 3 and col. 7, lines 56-59, which discloses, "a first counter is incremented as each unit of data is transferred to bi-directional buffer 340"** ;

issuing a read channel instruction to decrement the read channel count upon processing of received inbound data by the PU **(see col. 7, lines 59-60, which discloses, "and decremented as each unit of data is removed from bi-directional buffer 340")**;

incrementing a write channel count upon receipt of outbound data from the PU by the ED **(see col. 7, lines 62-66, which discloses, "A second counter is incremented as each unit of data is transferred to bi-directional buffer 345 and decremented as each unit of data is removed from bi-directional buffer 345. A value of zero in the second counter indicates that channel 303 is ready for use". See fig. 3, which discloses the buffer being bi-directional, which indicate that the counter is being incremented for each outbound data that's going into the buffer)**;

issuing a write channel instruction to decrement the write channel count upon transmission by the PU of the outbound data to the ED **(see col. 7, lines 63-64, which discloses, "and decrement as each unit of data is removed from bi-directional**

buffer". See also col. 7, lines 17-18, which discloses, "at the same time that data is being received from SCSI bus 120 by buffer 345");

accessing the read channel count **(see col. 7, lines 56-59 for accessing the real channel count (the first counter))**; and

comparing the accessed read channel count with a predetermined range to determine whether the PU has received data from the ED **(see col. 7, line 66 to col. 8, line 4, which discloses "Thus, when direction controller 360 receives a request for use of one of the bi-directional data channels, controller 360 examines the value of each of the counters to determine whether a channel is available. If a channel is available, controller 360 configures direction multiplexer 361 appropriately")**.

Young fail to specifically disclose that a FIFO or a buffer is a register.

Stuber discloses a FIFO or a buffer is a register **(See col. 6, lines 10-15, which discloses "FIFO 52 is a register that stores commands for retrieval on a first-in, first-out basis. Counter 62 maintains a count of the number of commands in FIFO 52. The count in counter 62 is incremented with each new command written into command queue 52 and is decremented with each command issued to device controller 50").**

Young (US pat. 6,408,354) and Stuber et al. (US pat. 6,801,972) are analogous art because they are from the same field of endeavor of using a counter and a FIFO to track data between a processing unit and external device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a parallel host adapter that interfaces two I/O buses includes at least two data channels that can be used concurrently as a receive data channel and a send data channel, or

alternatively, in one embodiment, as two receive channels as described by Young and a monitoring the slave device's behavior to bus transactions so that the slave device can either stall or split transactions, depending on the type of transaction, in the event it is in a shut down or initializing state as taught by Stuber.

The motivation for doing so would have been because Stuber teaches, **"Consequently, prior to the present invention, it was common to operate the slave device to stall the bus if its fed device shuts down. This solution stalled the entire bus system, rendering it unavailable to all users. The present invention is directed to a technique whereby non-locked transfer commands received when the fed device is shut down and during slave device re-initialization are split, rather than stalled" (see col. 5, lines 53-57).**

Therefore, it would have been obvious to combine Stuber et al. (US pat. 6,801,972) with Young (US pat. 6,408,354) for the benefit of creating the method to obtain the invention as specified in claims 20 and 35.

13. As per **claims 21 and 29**, the combination of Young and Stuber discloses "the method as recited in claim 20" **[See rejection to claim 20 above]**, Young further

discloses, comprising associating an active channel with the read register and the write register **(see col. 7, line 66 to col. 8, line 4).**

14. As per **claims 22 and 30**, the combination of Young and Stuber discloses "the method as recited in claim 21" **[See rejection to claim 21 above]**, Young further discloses wherein issuing a write channel instruction further comprises writing data externally to the PU **(see col. 7, lines 63-64 and col. 7, lines 17-18)**.

15. As per **claims 23 and 31**, the combination of Young and Stuber discloses "the method as recited in claim 21" **[See rejection to claim 21 above]**, Young further discloses wherein issuing a write channel instruction further comprises writing data to an internal register of the PU **(see col. 7, lines 63-64 and col. 7, lines 17-18)**.

16. As per **claims 24 and 32**, the combination of Young and Stuber discloses "the method as recited in claim 21" **[See rejection to claim 21 above]**, Young further discloses wherein issuing a read channel instruction further comprises returning read data to a PU dataflow **(see col. 7, line 65 to col. 8, line 4)**.

17. As per **claims 25 and 33**, the combination of Young and Stuber discloses "the method as recited in claim 20" **[See rejection to claim 20 above]**, Young further discloses, comprising associating a passive channel with the read register and the write register **(see fig. 2, which discloses a connection, such as a passive channel,**

between the FIFOs 240 and 245).

18. As per **claims 26 and 34**, the combination of Young and Stuber discloses "the method as recited in claim 25" **[See rejection to claim 25 above]**, Young further discloses wherein issuing a write channel instruction further comprises storing write data locally **(storing in the buffer 345)** for an external read operation **(see col. 7, lines 17-18, which discloses, "at the same time that data is being received from SCSI bus 120 by buffer 345")**.

19. As per **claims 27 and 35**, the combination of Young and Stuber discloses "the method as recited in claim 25" **[See rejection to claim 25 above]**, Young further discloses wherein issuing a read channel instruction further comprises returning read data to a PU dataflow **(see col. 7, lines 14-20)**.

(20) Response to Argument

As per Appellant's arguments, on page 12, regarding Young does not teach "incrementing a write channel count upon receipt of outbound data from the PU by the ED" is not persuasive.

This argument is not persuasive because fig. 3 of Young discloses a bi-directional data channel 303 functioning as a processing unit in communication with an external device (SCSI module 230), which is equivalent to Applicant's teachings regarding an 'external device (ED) and processing unit. Also, col. 7, lines 62-63

discloses, "A second counter is incremented as each unit of data is transferred to bi-directional buffer 345". **See fig. 3, which discloses the buffer being bi-directional. The buffer's counter is being incremented for each outbound data that's going into the buffer.** As also discloses in col. 7, lines 65-66, "a value of zero in the second counter indicates that channel 303 is ready for use". In other words, the buffer count increases when data is transferring into the buffer. That data converts to an 'outbound' data, since the buffer is bi-directional. As disclosed in fig. 3, whereas data is also moving from 251C to the buffer 345.

Further, applicant argues "Young teach incrementing the write channel . . . by the **write register** . . . however, the unique invention embodied therein recites 'incrementing a write channel . . . **by the ED** . . . therefore cannot support a rejection under Section 103 . . .". Examiner maintains that Young's teachings of incrementing the write channel by the **write register** is equivalent to applicant's claim language regarding incrementing by the **ED**, since Young's write register is inside of Young's PU. Therefore the teachings are synonymous.

(21) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Examiner
/Ernest Unelus/

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WQAS, TC2100, WG2180